What are claimed are:

1. A method of manufacturing thin film transistors comprising the steps of:

(a) forming a plurality of island-shaped semiconductor layers on a substrate having an insulative surface;

(b) implanting dopant into first regions at outsides of a region designated for a channel region in each of said semiconductor layers directly or through a thin insulation film whose thickness is equal to or less than 50 nm by ion implantation to form lightly doped regions; and

(c) implanting dopant into regions at outsides of said first regions in each of said semiconductor layers directly or through said thin insulation film to form heavily doped source/drain regions whose impurity concentration is higher than that of said lightly doped regions.

2. The method of manufacturing the thin film transistors according to claim 1, wherein said ion implanting steps (b) and (c) are carried out using an apparatus for non-mass-analyzed ion implantation which uses an ion source comprising a filament which emits thermal electrons.

3. The method of manufacturing the thin film transistors according to claim 2, wherein said ion implanting steps (b) and (c) are carried out with acceleration energy equal to or less than 30 keV.

4. The method of manufacturing the thin film transistors according to claim 2, wherein said ion implanting steps (b) and (c) are carried out using a hydride of a dopant element as an ion source.

5. The method of manufacturing the thin film transistors according to claim 1, wherein said step (a) comprises the substeps of:

(a-1) depositing an amorphous semiconductor layer on said substrate; and

(a-2) irradiating a layer beam on said amorphous semiconductor layer, to change said amorphous semiconductor layer into a crystalline semiconductor layer.

6. The method of manufacturing the thin film transistors according to claim 3 further comprising the step of;

(d) after said step (c), irradiating a laser beam onto said lightly doped regions and said source/drain regions directly or through said thin insulation film to activate impurities and recover damages caused by the ion implantation.

7. The method of manufacturing the thin film transistors according to claim 4 further comprising the steps, before said steps (b) and (c), of:

(e) forming an insulation layer and an electrode layer, covering said semiconductor layers; and

(f) patterning said electrode layer and said insulation layer to form gate electrodes and gate insulation films on the channel regions so that each of said semiconductor layers is partially exposed at both sides of each of said gate insulation film,

wherein said ion implanting step (b) is carried out while using said patterned gate insulation films and gate electrodes as a mask.

8. The method of manufacturing the thin film transistors according to claim 7,

wherein said gate insulation films have a thickness of equal to or greater than 50 nm, and said gate electrodes have a thickness of equal to or greater than 200 nm.

9. The method of manufacturing the thin film transistors according to claim 8, wherein said patterning step (f) patterns edges of each of said gate electrodes retarded from edges of associated one of said gate insulation films.

10. The method of manufacturing the thin film transistors according to claim 7, further comprising, before said step (e) and after said step (f), the step of;

(g) forming a shield on side walls of said gate electrode and said gate insulation film, while covering part of said lightly doped region.

11. The method of manufacturing the thin film transistors according to claim 10, wherein said step (g) comprises the substeps of:

(g-1) depositing a shield layer on said substrate, covering said gate electrode; and

(g-2) anisotropically etching said shield layer to remove the shield layer on flat surfaces, while leaving said shield on the side walls.

12. The method of manufacturing the thin film transistors according to claim 10, further comprising, after said step (c), the step of;

(h) removing said shield.

13. The method of manufacturing the thin film transistors according to claim 7, wherein said ion implanting steps (b) and (c) use hydride of dopant element as ion source and are carried out onto bare surfaces of said semiconductor layers or

through natural oxide films of a thickness equal to or less than approximately 5 nm under such conditions that concentration of hydrogen ions passing through said gate insulation films and reaching said semiconductor layers, is equal to or less than 10^{17} cm^{-3}.

14. The method of manufacturing the thin film transistors according to claim 1, wherein said substrate is a transparent substrate, comprising, before said step (a), the steps of:

(i) forming gate electrodes on said substrate; and

(j) forming a transparent gate insulation film on said substrate covering said gate electrodes.

15. The method of manufacturing the thin film transistors according to claim 14, further comprising, after said step (a) and before said steps (b) and (c), the steps of:

(k) forming a photoresist layer on said substrate, covering said semiconductor layer;

(l) exposing said photoresist layer from a rear surface of said substrate, using said gate electrode as a mask; and

(m) developing said exposed photoresist layer, to form a mask for ion implantation.

16. A method of manufacturing thin film transistors comprising the steps of:

(a) depositing an underlying insulation layer onto a glass substrate;

(b) depositing an amorphous silicon layer onto said underlying insulation layer;

(c) irradiating an eximer laser beam onto said amorphous silicon layer to convert said amorphous silicon layer into a polysilicon layer;

(d) patterning said polysilicon layer to form a plurality of island-shaped polysilicon layers;

(e) forming lamination including a lower insulation layer and an upper conductive layer on said glass substrate, covering said island-shaped polysilicon layers;

(f) forming a first mask on said conductive layer;

(g) patterning said conductive layer and said insulation layer, using said first mask as a mask, to form a gate electrode and a gate insulation film on each of said island-shaped polysilicon layers;

(h) implanting dopant lightly into said polysilicon layers, using said gate electrodes and said gate insulation films as a mask to form lightly doped regions;

(i) forming a second mask on side walls of each of said gate electrodes and gate insulation films, covering each of said polysilicon layers partially;

(j) implanting ions into said polysilicon layers, using said second mask as a mask, to form heavily doped source/drain regions whose impurity concentration is higher than that of said lightly doped regions;

(k) removing said second mask; and

(l) irradiating an eximer laser beam onto said lightly doped regions and said source/drain regions to activate impurities and recover damages caused by the ion implantation.

17. The method of manufacturing the thin film transistors according to claim 16, wherein said ion implanting steps (h) and (j) are carried out with acceleration energy of equal to or less than 30 keV.

18. Thin film transistors comprising:

a substrate having an insulative surface;

a plurality of island-shaped crystalline silicon layers formed on said substrate;

gate insulation films formed at a center of said crystalline silicon layer;

lightly doped regions formed in said crystalline silicon layers outwards from edges of said gate insulation film;

pairs of heavily doped source/drain regions, whose impurity concentration is higher than that of said lightly doped regions, formed in said crystalline silicon layers outwards from edges of said pair of lightly doped regions; and

gate electrodes formed on said gate insulation films, whose edges are retarded from edges of said gate insulation film.

19. The thin film transistors according to claim 18, wherein an area in said crystalline silicon layers under said gate electrode includes hydrogen atoms at a concentration equal to or less than 10^{17} cm^{-3}.

20. The thin film transistors according to claim 18, wherein said gate insulation films have a thickness of equal to or greater than 50 nm, and said gate electrodes have a thickness of equal to or greater than 200 nm.

21. The thin film transistors according to claim 18, wherein said plurality of island-shaped crystalline silicon layers includes areas for n-channel transistors and areas for p-channel transistors, said lightly doped regions are formed only in the areas for said n-channel transistors.